U.S. Patent Application For

A METHOD FOR FORMING CONDUCTORS IN SEMICONDUCTOR DEVICES

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The present invention relates generally to semiconductor devices; and more particularly relates to methods and apparatus for forming digit lines of improved conductivity, such method having particular usefulness in the fabrication of memory devices, and particularly to memory devices having programmable elements accessible by a diode.

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Background of the Invention

Diode arrays are well known memory storage arrays used in semiconductor memory devices. A selected diode is typically addressed via digit line and word line selection. A resistance of a programmable resistor in series with the selected diode is controlled to select a desired memory state. In one case the programmable resistor may be an ovonic element, such as a chalcogenide material. The internal structure of the chalcogenide is modified to alter its resistance and therefore its "logic" state. The modification of the structure is ovonic and is dependent on the current which is applied to the element through the diode. It is desirable to reduce stray resistance which may be in series with the diode, since by reducing the stray resistance the ovonics can be more closely controlled with less current, thereby reducing power requirements.

A Method For Forming Conductors In Semiconductor Devices By Gonzalez et al.

Summary of the Invention

The invention includes a method and apparatus for forming a semiconductor device wherein a conductive element within the substrate is strapped by another conductive layer above. In one currently envisioned embodiment, another conductive layer will be interposed between the substrate and the strapping layer. In one exemplary preferred implementation, the semiconductor device will be a memory device comprising a diode serially connected to a programmable resistor. The diode is in electrical communication with a buried digit line. An electrically conductive plug is electrically interposed between the digit line and a strapping layer, thereby creating a double metal structure wherein the strapping layer is a second metal layer overlying metal wordlines.

In a method of a first embodiment, the strapping material is electrically connected to the digit line through a planar landing pad overlying the conductive plug. An insulative material is sloped to the planar landing pad in order to provide a surface conducive to the formation of the strapping material. Typically a layer of titanium silicide is formed on the buried digit line.

In an exemplary method of forming a second embodiment in accordance with the present invention, diodes are formed, each having a maximum width equal to f, which may be equal to the minimum photolithographic limit of the photolithographic equipment being used, and distanced one from the other along a length of the digit line by a maximum distance equal to f; at least portions of the diodes are masked; at least a portion of an insulative material interposed between two diodes is removed to expose the buried digit line; and the conductive plug is formed in contact with the exposed portion of the buried digit line. After the formation of a programmable resistor in series with the diode a wordline is formed in electrical communication

Page 3

A Method For Forming Conductors In Semiconductor Devices By Gonzalez et al.

H: 116339 (2HRN011.DOC)

with each of the programmable resistors, and an insulative layer is formed overlying each wordline. Next an insulative spacer layer is deposited and etched to expose the conductive plug. The strapping layer is then formed overlying and in contact with the conductive plug.

5   In the second embodiment the width of the diode is equal to f and the electrically conductive plug is formed within a distance f from a sidewall of the diode. An electrically insulative spacer is interposed between the plug and the sidewall of the diode. In this embodiment the diode and the plug are made of polycrystalline silicon, although it is possible to use any conceivable diode structure, for example a metal/semiconductor. In the second

10   embodiment the cathode of the diode is fabricated in the substrate and the anode is fabricated overlying the substrate or vice versa.

         In the typical memory array of the invention the programmable resistor is ovonic and the array is a mesa type structure. The diodes are either planar or container structures.

15   The invention provides redundancy since the digit line is a buried component and the strapping layer is an upper component. Thus, even if the metal of the strapping layer breaks, operation of the memory device is maintained through the buried digit line. Thus the device has better electromigration reliability, and there is no memory disturbance from cell to cell due to the

20   collection of current in the digit line.

         There is space savings when using the structure of the second embodiment, since the area between cells is no longer just isolation space but is used instead for contact to the buried digit line, thereby providing efficient spacing of the cell for high compaction while at the same time.

25   providing good cell to cell isolation.

By using the double metal scheme of the invention the series resistance to the diode is
reduced to the diode/programmable resistor structure. This resistance is decreased even further
by providing a strapped conductive plug for every two diodes of the array and physically
5   interposed therebetween. By using Titanium silicide on the buried digit line in conjunction with
the strapped metal layer the best packing density is achieved with minimal processing steps. In
addition the titanium silicide is used to minimize the number of connections needed to connect
the strapping material and buried digit line.

Brief Description of the Drawings

Figure 1A is a cross sectional view of a substrate in which digit lines have been formed.
The cross sectional view of Figure 1A is taken through the width of the digit lines.

15   Figure 1B is a cross sectional view taken through the length of one of the digit lines
shown in Figure 1A.

Figures 2A and 2B are the cross sectional view shown in Figure 1B following depositions
of silicon dioxide and polycrystalline silicon.

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Figures 3A and 3B are the cross sectional views shown in Figures 2A and 2B,
respectively, following a CMP.

Figure 4 is the cross sectional view of Figure 3A following a doping of the
25   polycrystalline silicon.

A Method For Forming Conductors In Semiconductor Devices By Gonzalez et al.

Figure 5 is the cross sectional view of Figure 4 following the formation of a contact plug.

Figure 6 is a cross sectional view of Figure 5 following the formation of programmable resistors, word lines and a landing pad.

Figure 7 is a cross sectional view of Figure 6 following the formation and etch of an oxide layer.

Figure 8 is a cross sectional view of Figure 7 following the formation of a strapping layer.

Figure 9A is a cross sectional view of a substrate in which digit lines have been formed. The cross sectional view of Figure 9A is taken through the width of the digit lines.

Figure 9B is a cross sectional view taken through the length of one of the digit lines shown in Figure 9A.

Figure 10A is a cross sectional view of a the substrate of Figure 9B following the deposition, planarization and masking of an oxide layer.

Figure 10B is a top planar view of Figure 10A.

Figures 11A and 11B are the cross sectional views of Figures 9A and 9B, respectively, following the formation of polycrystalline silicon regions in the oxide layer of Figures 10A and 10B.

Page 6

A Method For Forming Conductors In Semiconductor Devices By Gonzalez et al.

Figure 12A is the cross sectional view of Figure 11B following the masking of the polycrystalline silicon regions and the oxide layer and following the etching of the oxide layer in unmasked regions.

Figure 12B is a top planar view of Figure 12A.

Figure 13 is a cross sectional view of Figure 12A following removal of a masking layer and deposition of a spacer layer.

Figure 14 is the cross sectional view of Figure 13 following the etching of the spacer layer to form spacers adjacent to sidewalls of the polycrystalline silicon regions.

Figure 15 is the cross sectional view of Figure 14 following a deposition of polycrystalline silicon.

Figure 16 is the cross sectional view of Figure 15 following a CMP.

Figure 17A is the cross sectional view of Figure 16 following the formation of ovonic devices.

Figure 17B is the cross sectional view of Figure 16 following the formation of ovonic devices in a recess of a nitride layer.

A Method For Forming Conductors In Semiconductor Devices By Gonzalez et al.

Figures 18A and 18B are the cross sectional views of Figures 17A and 17B, respectively, following the deposition of a conductive layer and an oxide layer and the masking thereof.

Figures 19A and 19B are the cross sectional views of Figures 18A and 18B, respectively, following removal of exposed portions of the conductive layer and the oxide layer and the mask of Figures 18A and 18B.

Figures 20A and 20B are the cross sectional views of Figures 19A and 19B, respectively, following the deposition of an oxide layer.

Figure 21A and 21B are the cross sectional views of Figure 20A and 20B, respectively, following etching of the oxide layer of Figures 20A and 20B and the deposition of a strapping layer.

Brief Description of the Preferred Embodiments

The invention is described in reference to the exemplary embodiment of a memory device comprising a diode serially connected to a programmable resistor. The diode is in electrical communication with a buried digit line. An electrically conductive plug is electrically interposed between the digit line and a strapping layer, thereby creating a "double metal" structure wherein the strapping layer is a second metal layer overlying metal wordlines.

In an exemplary memory array the programmable resistor includes an ovonic element and the array is a mesa type structure. Alternately, in a read only memory structure, the

A Method For Forming Conductors In Semiconductor Devices By Gonzalez et al.

programmable resistor may be an anti-fuse device. The diode is either a planar or a container structure, and is used as a setting device to control current to the programmable resistor.

The method of the first embodiment is discussed relative to Figures 1A-8. Figure 1A depicts a p-type substrate 5 which was masked with a pattern which defined active areas. Field oxide 6 was then grown to electrically isolate the active areas, and the mask was removed. The exposed portions of the substrate 5 are implanted at a dose of 1-9E^{13} with a dopant such as phosphorous having an energy of 100-150 KeV to create n- regions 7 in the active area of the substrate. Titanium is deposited and a RTP sinter is performed during which the titanium reacts with the exposed portions of the silicon substrate to form titanium silicide 8. Unreacted portions of the titanium are removed with a low temperature piranha etch. The titanium silicide regions 8 and the n- region of the substrate 7 form the buried digit lines 10. One of the digit lines 10 is shown in longitudinal cross-section in Figure 1B, while Figure 1A depicts the entire column pattern in vertical cross-section lateral to the digit lines 10.

The titanium silicide 8 remaining following the piranha etch is masked (mask not shown) to protect titanium silicide 8 in future contact areas during an etch which removes the titanium silicide 8 in unmasked regions. The masked is then removed (see Figure 1B).

Figures 2A and 2B depict the cross sectional view shown in Figure 1B following further process steps. In Figure 2A a relatively thick layer of silicon dioxide 15 is deposited to overlie the buried digit lines 10 and the field oxide 6, which is not shown in this cross section. The silicon dioxide 15 is masked with a contact pattern, not shown, defining polycrystalline silicon plugs and etched to create openings in which the polycrystalline silicon plugs may be formed. The openings expose the digit lines 10 in contact regions. After removal of the mask a layer of

A Method For Forming Conductors In Semiconductor Devices By Gonzalez et al.

polycrystalline silicon 20 is deposited to fill the openings. The polycrystalline silicon 20 is

doped. The dopant is selected from materials having n- impurities such as phosphorous,

antinomy, and arsenic. The dopant may be implanted at 35-150 KeV and a dose of $3E^{13}$-$1E^{14}$.

The polycrystalline silicon 20 may be deposited in situ and doped between $1E^{16}$ and $1E^{18}$

5   atoms/cc or doped after the polycrystalline silicon 20 is deposited to the same dopant level.

In an alternate embodiment shown in Figure 2B the silicon dioxide 15 is masked and

etched as in Figure 2A. Following the etch of the silicon dioxide 15 the substrate is implanted

with a dopant selected from materials having p- impurities, such as boron, gallium, and BF_2 to

form p- regions 17. The dopants have energies ranging from 50-100 KeV and dosages of

$1E^{13}$-$1E^{14}$ atoms/cm^2 The polycrystalline silicon 20 is then deposited to fill the openings. In this

embodiment the polycrystalline silicon 20 is implanted or in situ doped with a dopant selected

from materials having p+ impurities, such as boron, gallium, and BF_2, to create a p+

polycrystalline silicon 20. The dopants have energies ranging from 35-50 KeV and dosages of

15     $1E^{15}$ to $5E^{15}$ atoms/cm^2.

Figures 3A and 3B are the cross sectional views shown in Figures 2A and 2B,

respectively, following further process steps. In Figures 3A and 3B the polycrystalline silicon

layer 20 of Figures 2A and 2B, respectively, have been planarized, such as through chemical

20   mechanical planarization (CMP) to remove portions of the polycrystalline silicon 20 overlying

the silicon dioxide 15, while at the same time retaining the polycrystalline silicon 20 in the

openings. The CMP is selective to the silicon dioxide 15. Thus the CMP action stops when the

silicon dioxide 15 is exposed. In Figure 3B the p+ polycrystalline silicon 20 and the p- region 17

together form a diode 30 with the digit line 10.

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Figure 4 is the cross sectional view of Figure 3A following further process steps. In Figure 4 a p+ implant and an activation cycle, which includes a rapid thermal process (RTP) cycle and hydrogen cycle, has been performed to create a p+ region 25 at an upper portion of the polycrystalline silicon 20 of Figure 3A. During the implant typical p-type dopants, such as

5   Boron, Gallium, and BF_2 are implanted at energy of 35-50 KeV and at a dosage of $1E^{15}$ to $5E^{15}$ atoms/cm^2. The lower portion of the polycrystalline silicon remains n- thereby forming a diode 30 vertical to the buried digit line 10. For simplicity the remaining steps of this embodiment will pertain to diode 30 of Figure 4 although the same steps would be applicable if the diode of Figure 3B were used instead.

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Next the silicon dioxide 15 and diodes 30 are masked (mask not shown), to pattern a contact to the digit line 10. The silicon dioxide 15 is etched to form openings (not shown) to expose the digit lines 10, and the resist used for masking is removed.

15   Figure 5 depicts the cross sectional view of Figure 4 following further process steps. In Figure 5 a thin layer of titanium and titanium nitride 35 is deposited along the sidewalls of the openings and overlying the digit lines 10. Tungsten 40 is deposited to fill the opening and to overly the titanium. The titanium and titanium nitride 35 and tungsten 40 are chemically mechanically planarized to expose the silicon dioxide 15 and form a contact plug 45.

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Figure 6 depicts the cross sectional view of Figure 5 following further process steps. In Figure 6 at least one layer has been deposited, masked and etched to form programmable elements 50 (such as ovonic elements or antifuse elements) overlying each diode 30. In the case where an ovonic device is formed several deposition, mask, and etch steps may be utilized to

layer Titanium tungsten, carbon, a first nitride layer, chalcogenide, and a second nitride layer. Various methods can be used when forming the ovonic device.

A first metal layer or stack of approximately 5000 Angstrom is then deposited to overly the silicon dioxide 15, programmable resistors 50 and the contact plug 45. The metal layer is then patterned with a mask, not shown, and etched to form wordlines 60 in contact with the programmable resistors 50 and a planar landing pad 65 overlying the contact plug 45. The mask is then removed.

Figure 7 is a cross sectional view of Figure 6 following further process steps. In Figure 7 an interlevel dielectric oxide layer 70 is deposited, chemically mechanically planarized to create a planar surface, patterned, etched with a wet oxide 7:1 hydrofluoric dip for 15 seconds, and dry etched to expose the landing pad 65. The etch of the invention creates an opening 75 in the oxide 70 having a sloped sidewall 80. The direction of the slope is such that the upper portion of the opening has a larger perimeter than that of the lower portion.

Figure 8 is a cross sectional view of Figure 7 following further process steps. In Figure 8 a second metal layer or stack, which is well known to those skilled in the art, is deposited to overlie the oxide 70 and the landing pad 65. The sloped sidewalls 80 are conducive to good step coverage during the deposit of the second metal layer. Substantially vertical sidewalls 80 may be employed for tighter geometries. The second metal layer is patterned with a mask and etched to define and form a strapping layer 85. The mask is then removed. Although this cross section shows one strapping layer 85 in electrical communication with one landing pad 65 through one contact plug 45, it should be noted that a plurality of contact plugs 45 and landing pads 65 may be in electrical communication with the digit line 10 and the strapping layer 85 at a plurality of

A Method For Forming Conductors In Semiconductor Devices By Gonzalez et al.

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points to further reduce the resistance in series with the diodes 30. In addition, it should also be remembered that there are a plurality of digit lines formed along other cross sections.

In a method of a second embodiment diodes are formed, each having a maximum width equal to f, which is equal to the minimum photolithographic limit of the photolithographic equipment being used, and distanced one from the other along a length of the digit line by a maximum distance equal to f; at least portions of the diodes are masked; at least a portion of an insulative material interposed between two diodes is removed to expose the buried digit line; and the conductive plug is formed in contact with the exposed portion of the buried digit line. After the formation of a programmable resistor in series with the diode a wordline is formed in electrical communication with each of the programmable resistors, and an insulative layer is formed overlying each wordline. Next an insulative spacer layer is deposited and etched to expose the conductive plug. The strapping layer is then formed self-aligned to the conductive plug.

In this embodiment the diode and the plug are made of polycrystalline silicon, although it is possible that any conceivable diode structure may be used. In the second embodiment the P portion of the diode is fabricated in the substrate and the N portion is fabricated overlying the substrate.

In an enhancement of the second embodiment a buried digit line is strapped at each memory cell to reduce the series resistance thereby creating greater drive. The self alignment feature of the invention facilitates a denser array.

The second embodiment of the invention is depicted in Figures 9A- 21B.

Page 13

A Method For Forming Conductors In Semiconductor Devices By Gonzalez et al.

In Figure 9A p- digit lines 100 have been formed in an n- substrate 105 according to methods known in the art. The present embodiment is shown with LOCOS isolation having field oxide regions 110, but is adapted to trench isolation and modified LOCOS.

Figure 9B is a longitudinal cross section through the length of one of the digit lines 100 shown in lateral cross-section in Figure 9A.

Figure 10A is a cross sectional view of a the substrate of Figure 9B following further process steps. In Figure 10A a conformal silicon dioxide layer 115 is deposited and planarized, preferably with CMP. The depth of the silicon dioxide layer 115 is selected to be greater than the desired height of future electrical contact plugs to digit lines 100. The silicon dioxide layer 115 is patterned with a photoresist mask 120 to define the electrical contact plugs. Openings are etched in the exposed portions of the silicon dioxide layer 115 to expose the digit lines 100. By using the method of the invention it is possible to have the minimum width of both the masked and unmasked regions along the length of the digit line equal to f. Thus the method of the invention allows the fabrication of a dense memory array.

Figure 10B is a top planar view of the device of Figure 10A. Since the digit lines underlie the photoresist mask 120 and silicon dioxide layer 115 they are outlined by dashed lines which also define active areas. The field oxide region underlies the silicon dioxide and lies between two digit lines.

Figures 11A and 11B deposit the cross sectional views of Figures 9A and 9B, respectively, following further process steps. In Figures 11A and 11B the openings have been

A Method For Forming Conductors In Semiconductor Devices By Gonzalez et al.

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filled with N+poly using standard fill techniques. The N+ poly is planarized preferably using CMP. The N+ poly forms contact plugs 125 to the digit lines 100, and the positive N+ electrode 130 of the diode is formed from out diffusion of the N type dopant from the N+ poly, thereby avoiding leakage current because the diode behaves as a single crystal diode.

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Figure 12A depicts the cross sectional view of Figure 11B following further process steps, and Figure 12B is a top planar view of the device of Figure 12A. In Figures 12A and 12B the contact plugs 125 and silicon dioxide 115 shown in Figures 11A and 11B are patterned with a mask 135, and the silicon dioxide 115 is etched in unmasked areas to form openings 140 to expose the digit lines 100 in the unmasked areas. The mask 135 may be misaligned with the contact plugs 125 since the method creates self aligned openings between the contact plugs 125. In one embodiment each opening eventually allows the strapping layer to be in electrical contact to the digit line 100 at each memory cell thereby decreasing series resistance to allow for a higher programming current to adequately set the logic state of a chalcogenide material in an ovonic device which will be fabricated overlying each of the contact plugs 125.

However, the masking may be more selective in order to form fewer openings 140.

Figure 12 B, as in Figure 10B, the digit lines have been outlined with dashed lines. In addition portions of contact plugs 125 underlying mask 135 are shown with dotted lines.

Figure 13 is a cross sectional view of Figure 12A following further process steps. In Figure 13 the mask 135 has been removed and an oxide spacer layer 145 deposited.

A Method For Forming Conductors In Semiconductor Devices By Gonzalez et al.

Figure 14 is a cross sectional view of Figure 13 following further process steps. In Figure 14 the oxide spacer layer has been anisotropically dry etched to form spacers 150 on the sidewalls of the contact plug 125. A P+ region 155 is formed in the exposed portion of the digit line 100 during a shallow P+ implant, using a dopant from the group consisting of BF 2 and at an energy equal to 25-75 KeV and a dosage equal to $5E^{14}$-$5E^{15}$ atoms/cm^2 , to lower the resistance of a future metal interconnect. During the implant it is necessary to protect the n+ contact plug 125 with some form of mask (not shown) such as a hand mask.

Figure 15 is a cross sectional view of Figure 14 following further processing steps. In Figure 15 a layer of polycrystalline silicon 165 is deposited.

Figure 16 is a cross sectional view of Figure 15 following further processing steps. In Figure 16 the contact plugs 125, spacers 150, and polycrystalline silicon 165 are CMPed to create a planar surface and to eliminate portions of spacer 150 having non uniform thicknesses. The spacers 150 following the CMP process provide greater isolation properties than did the spacers existing before CMP.

The polycrystalline silicon layer 165 forms a planar landing pad 170 following the CMP. A digit line strapping layer may be fabricated overlying the landing pad 170 as is explained below. The polycrystalline silicon 165 is doped P+ using a P+ implant subsequent to the planarization step.

In one alternate embodiment which is shown in Figure 17A the contact plugs 125 are fabricated to be larger than the photolithographic limit. Figure 17A is similar to Figure 16 except that the contact plugs 125 are larger and further processing steps have been performed. An

A Method For Forming Conductors In Semiconductor Devices By Gonzalez et al.

ovonic device 175 is fabricated overlying each of the contact plugs 125 according to a method of layer fill and etching back according to a pattern (not shown) defining the ovonic device 175. The width of the ovonic device may be as small as the photolithographic limit thereby allowing more access to the landing pad 170. In this embodiment the ovonic device consists of the

5　following layers: tungsten 176, a lower TiN or TiC_xN_y layer 177, a nitride layer 182, a chalcogenide layer 178, and an upper TiN layer 179. A pore opening 183 is created in the nitride layer 182 and the chalcogenide layer 178 fills the pore opening 183. In this method the chalcogenide material is applied using conventional thin film deposition methods and the other materials of the ovonic devices 175 are formed with various methods of layering and etching.

Typical chalcogenide compositions for these memory cells include average concentrations of Te in the amorphous state well below 70%, typically below about 60% and ranging in general from as low as about 23% up to about 56% Te, and most preferably to about 48% to 56% Te. Concentrations of Ge are typically above about 15% and range from a low of about 17% to about 44% average, remaining generally below 50% Ge, with the remainder of the principal constituent elements in this class being Sb. The percentages given are atomic percentages which total 100% of the atoms of the constituent elements. In a particularly preferred embodiment, the chalcogenide compositions for these memory cells comprise a Te concentration of about 55%, a Ge concentration of about 22%, and a Sb concentration of about

20　22%. This class of materials are typically characterized as $Te_aGe_bSb_{100-(a+b)}$, where a is equal to or less than about 70% and preferably between about 60% to about 40%, b is above about 15% and less than 50%, preferably between about 17% to about 44%, and the remainder is Sb.

Page 17

A Method For Forming Conductors In Semiconductor Devices By Gonzalez et al.

An electrically insulative nitride layer 180 is deposited overlying the ovonic device 190. The nitride layer is patterned in order to expose at least a portion of the upper surface 181 of the ovonic device 175.

5   Figure 17B is a cross sectional view of Figure 16 following further processing steps. An ovonic device 190 is fabricated by a second method. When using the second method it is necessary to deposit a nitride layer 185 or a combination silicon dioxide layer with an overlying nitride layer instead of the silicon dioxide layer 115. openings (not shown) are etched partially into the nitride layer 185 or the nitride of the nitride-silicon dioxide combination layer. Recessed

10   ovonic devices 190 are then fabricated in the openings overlying the contact plugs 125. The fabrication comprises a layering, which includes deposition fill and etching back, of the following materials in the sequential order in which they are written: tungsten 191, a lower TiC_xN_y layer 192, chalcogenide layer 193, and an upper TiC_xN_y layer 194. By using this method the chalcogenide material fills the hole without patterning.

15   Next wordlines are created. Figures 18A and 18B are the cross sectional views of Figures 17A and 17B, respectively, following the formation of a conformal conductive layer 200 in electrical contact with the ovonic devices 175 and 190, respectively. Typically the conductive layer 200 is a deposit of aluminum, copper, gold, silver, or refractory metals. An oxide layer 205

20   is then formed overlying the conductive layer 200. The wordlines are patterned with a mask 210 overlying the oxide layer 205, and exposed portions of the oxide layer 205 are removed during a first etch, and then exposed portions of the conductive layer 200 are removed during a second etch. The portions of the conductive layer 200 remaining subsequent to the etch form the word lines 215, see Figures 19A and 19B, respectively.

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A Method For Forming Conductors In Semiconductor Devices By Gonzalez et al.

The mask is then removed, and a conformal oxide layer 220 is deposited, see Figures 20A and 20B, respectively.

In Figures 21A and 21B an oxide spacer 225 is formed to electrically insulate the wordlines 215 from a future strapping layer. The spacer 225 is formed by anisotropically etching of the oxide layer 220. The etch of the oxide layer 220 exposes the landing pads 170 in Figure 21B. In addition to the oxide layer 220 the nitride layer 180, in Figure 21A, is etched to expose the landing pads 170 shown in Figure 21A.

Further shown in Figures 21A and 21B is the strapping layer 230, typically aluminum, copper, or other conductive material, deposited in contact with the landing pad 170. The strapping layer is in electrical communication with the digit line 100 through the landing pad 170. Typically the strapping layer 230 is patterned to define desired interconnects and then etched according to the pattern. The photoresist (not shown) used for patterning is then removed and the metal is alloyed.

The invention provides redundancy since the digit line is a buried component and the strapping layer is an upper component. Thus, even if the metal of the strapping layer breaks, operation of the memory device is maintained through the buried digit line. Thus the device has better electromigration reliability, and there is no memory disturbance from cell to cell due to the collection of current in the digit line.

There is space savings when using the structure of the second embodiment, since the area between cells is no longer just isolation space but is used instead for contact to the buried digit.

A Method For Forming Conductors In Semiconductor Devices By Gonzalez et al.

line, thereby providing efficient spacing of the cell for high compaction while at the same time providing good cell to cell isolation.

By using the double metal scheme of the invention the series resistance to the diode is

5   reduced to the diode/programmable resistor structure. This resistance is decreased even further by providing a strapped conductive plug for every two diodes of the array and physically interposed therebetween. By using titanium silicide on the buried digit line in conjunction with the strapped metal layer the best packing density is achieved with minimal processing steps.

10   It should be noted that opposite doping may be used throughout the described embodiments without departing from the scope of the invention.

While the invention is susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in

15   detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

A Method For Forming Conductors In Semiconductor Devices By Gonzalez et al.

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